AMENDMENTS TO THE CLAIMS:

Please amend claims 4, 8, and 9 as indicated below. This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Original) A semiconductor device, comprising:

a first wiring structure formed on a semiconductor substrate and including a first plug and a first wiring formed on said first plug; and

a second wiring structure formed on said semiconductor substrate and including a second plug and a second wiring formed on said second plug;

wherein the upper surface of said first wiring is positioned higher than the upper surface of said second wiring, and the lower surface of said first wiring is positioned flush with or lower than the upper surface of said second wiring.

2. (Original) The semiconductor device according to claim 1, wherein said wiring layer is of a single layer structure or of a multi-layered structure, and said first and second wiring structures are formed adjacent to each other within the same wiring layer.

3. (Original) The semiconductor device according to claim 1, wherein each of said first and second wirings is surrounded by an insulating film.

4. (Currently Amended) The semiconductor device according to claim 3, wherein said

insulating film includes a first insulating film and a second insulating film formed on said first insulating film, said first and second plugs and said second wiring are buried in said first insulating film, and said ~~second~~ first wiring is buried in said second insulating film.

5. (Original) The semiconductor device according to claim 4, wherein said first and second insulating films are formed of different materials.

6. (Original) The semiconductor device according to claim 5, wherein said second insulating film is selected from the group consisting of a low dielectric constant film, an organic silicon oxide film and an inorganic silicon oxide film.

7. (Original) The semiconductor device according to claim 5, wherein each of said first and second insulating films is selected from the group consisting of a low dielectric constant film, an organic silicon oxide film and an inorganic silicon oxide film.

8. (Currently Amended) The semiconductor device according to claim 1, wherein each of said first and second plugs and said second wiring is surrounded by an insulating film, and said first wiring is ~~surrounded by a space~~ an air-bridge wiring .

9. (Currently Amended) The semiconductor device according to claim 1, wherein each of said first and second plugs and said first and second wirings is ~~surrounded by a space~~ an air-bridge wiring .

10. (Original) The semiconductor device according to claim 1, wherein the cross sectional area of said first wiring is larger than the cross sectional area of said second wiring.

11. (Original) The semiconductor device according to claim 1, wherein the wiring width of said first wiring is larger than the wiring width of said second wiring.

12. (Original) The semiconductor device according to claim 1, wherein the thickness of said first wiring is larger than the thickness of said second wiring.

13. (Original) The semiconductor device according to claim 1, wherein the distance between the mutually facing side surfaces of said first and second wirings is larger than 0 μm and not larger than 0.13 μm.

14. (Original) The semiconductor device according to claim 1, wherein satisfied is the inequality $1 < L2/L1 \leqq 13$, where L1 represents the distance between the mutually facing side surfaces of said first and second wirings, and L2 represents the width of said first wiring.

15. (Original) The semiconductor device according to claim 1, wherein satisfied are inequalities of $1 \leqq L2/L3 \leqq 10$ and $1 \leqq L5/L4 \leqq 10$, where L2 represents the width of said first wiring, L3 represents the size of said first plug in the width direction of said first wiring, L4 represents the size of said second plug in the width direction of said second wiring, and L5 represents the width of said second wiring.

16. (Original) The semiconductor device according to claim 1, wherein each of said first and second wirings is formed of an elemental metal selected from the group consisting of Cu, Al, W, Ag and Au or an alloy selected from the group consisting of Al-Cu, Al-Si-Cu and WSi or a polysilicon.

17. (Original) The semiconductor device according to claim 1, wherein, where each of said first and second wirings is formed of Cu or Al-Cu, each of said first and second wirings is provided with a barrier film or a liner film made of a material selected from the group consisting of Ti, TiN, Ta, TaN, and Ti/TiN, and where each of said first and second wirings is formed of Al, each of said first and second wirings is provided with a barrier film or a liner film made of a material selected from the group consisting of Nb and NbN.

18. (Original) The semiconductor device according to claim 1, wherein the lower portion of each of said first and second plugs is connected to any of the source region and the drain region of a MOS transistor formed on said semiconductor substrate.

19. (Original) The semiconductor device according to claim 1, further comprising a third plug, a third wiring formed on said third plug, a fourth plug and a fourth wiring formed on said fourth plug, wherein the upper surface of said third wiring is positioned higher than the upper surface of said fourth wiring, the lower surface of said third wiring is positioned flush with or lower than the upper surface of said fourth wiring, the lower portion of said first plug is connected to said third wiring, and the lower portion of said second plug is connected to said fourth wiring.

20. (Original) The semiconductor device according to claim 1, further comprising a third plug, a third wiring formed on said third plug, a fourth plug and a fourth wiring formed on said fourth plug, wherein the upper surface of said third wiring is positioned flush with the upper surface of said fourth wiring, the lower portion of said third plug is connected to the upper surface of said first wiring, and the lower portion of said fourth plug is connected to the upper surface of said second wiring.

21. (Original) A semiconductor device, comprising:

a first wiring structure formed on a semiconductor substrate and including a first plug and a first wiring formed on said first plug; and

a second wiring structure formed on said semiconductor substrate and including a second plug and a second wiring formed on said second plug;

wherein said first and second wiring structures constitute a wiring layer of an identical wiring level on said semiconductor substrate, and said first and second wiring structures are formed by using different materials.

22. (Original) The semiconductor device according to claim 21, wherein said first and second wirings are formed by using different materials.

23. (Original) The semiconductor device according to claim 21, wherein the upper surface of said first wiring is positioned higher than the upper surface of said second wiring, and the lower surface of said first wiring is positioned flush with or lower than the upper surface of

said second wiring, where said first wiring is formed of Ag or Au and said second wiring is formed of Cu.

cancelled

24. (~~Withdrawn~~) A method of manufacturing a semiconductor device, comprising:

forming a first insulating film on a semiconductor substrate;

selectively etching said first insulating film so as to form a first wiring trench on the surface of said first insulating film, a first contact hole extending through that portion of said first insulating film which is positioned between the bottom of said first wiring trench and the semiconductor substrate, and a second contact hole extending through said first insulating film;

burying a first conductive film in said first wiring trench, said first contact hole and said second contact hole;

forming a second insulating film on said first insulating film having said first conductive film buried therein;

selectively etching said second insulating film so as to form in said second insulating film a second wiring trench connected to said second contact hole and positioned substantially in parallel to said first wiring trench; and

burying a second conductive film in said second wiring trench.

cancelled

25. (~~Withdrawn~~) The method of manufacturing a semiconductor device according to claim 24, wherein the formation of said first wiring trench, said first contact hole and said second contact hole comprises:

forming a first mask pattern having a first open portion corresponding to said first wiring trench and a second open portion corresponding to said second contact hole on said first

insulating film;

forming a resist film on said first insulating film having said first mask pattern formed thereon;

forming on said resist film a second mask pattern having a third open portion corresponding to said first contact hole and a fourth open portion corresponding to said second wiring trench, the positions of said first open portion and said third open portion being aligned and the positions of said second open portion and said fourth open portion being also aligned so as to form said second mask pattern;

selectively etching said resist film with said second mask pattern used as a mask so as to form in said resist film a fifth open portion corresponding to said first contact hole and a sixth open portion corresponding to said second wiring trench;

selectively etching said first insulating film with said resist film and said first mask pattern used as a mask after removal of said second mask pattern so as to form said first and second contact holes in said first insulating film; and

selectively etching said first insulating film with said first mask pattern used as a mask after removal of said resist film so as to form said first wiring trench.

Cancelled

26. (~~Withdrawn~~) A method of manufacturing a semiconductor device, comprising:

forming a first insulating film on a semiconductor substrate;

selectively etching said first insulating film so as to form a first wiring trench on the surface of said first insulating film, a first contact hole extending through that portion of said first insulating film which is positioned between the bottom of said first wiring trench and the semiconductor substrate, and a second contact hole extending through said first insulating film;

burying a first conductive film in said first wiring trench, said first contact hole and said second contact hole;

forming a second insulating film on said first insulating film having said first conductive film buried therein;

selectively etching said second insulating film so as to form in said second insulating film a second wiring trench connected to said second contact hole and positioned substantially in parallel to said first wiring trench;

burying a second conductive film in said second wiring trench; and

removing said second insulating film positioned around said second wiring so as to leave said second wiring surrounded by a space.

cancelled

27. (~~Withdrawn~~) A method of manufacturing a semiconductor device, comprising:

forming a first insulating film on a semiconductor substrate;

selectively etching said first insulating film so as to form a first wiring trench on the surface of said first insulating film, a first contact hole extending through that portion of said first insulating film which is positioned between the bottom of said first wiring trench and the semiconductor substrate, and a second contact hole extending through said first insulating film;

burying a first conductive film in said first wiring trench, said first contact hole and said second contact hole;

forming a second insulating film on said first insulating film having said first conductive film buried therein;

selectively etching said second insulating film so as to form in said second insulating film a second wiring trench connected to said second contact hole and positioned substantially in

parallel to said first wiring trench;

burying a second conductive film in said second wiring trench;

removing said first and second insulating film positioned around said first and second plugs and around said first and second wirings so as to have said first and second plugs and said first and second wirings surrounded by a space.